Roll No. | | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 09

B.Tech.(EE) PT (Sem.–3)

DIGITAL ELECTRONICS

Subject Code : BTEE-404

M.Code : 72164

Time : 3 Hrs. Max. Marks : 60

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students has to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students has to attempt any TWO questions.**

SECTION-A

1. Answer briefly :

a) What is the difference between a latch and a flip-flop?

b) How do you specify the delay in VHDL?

c) What is meant by a bit?

d) Which gates are called as universal gates and what are their advantages?

e) What are the fundamental properties of Boolean algebra?

f) What are minterm and maxterm?

g) What are the limitations of the Karnaugh map?

h) What do we need to generate hardware from VHDL model?

i) Write down the duality theorem.

j) What is meant by Checksum?

SECTION-B

2. Explain interface between TTL to CMOS circuit.

3. Design a 4-bit BCD adder using full adder and explain its structure and compute the circuit to add 1001 and 0101. Write the sum and carry outputs of the given binary number.

4. Select a 4096 × 8 bit ROM memory to store a program. The memory chip has two chip select inputs and operates from a 5V d.c. power supply. How many pins are needed for the integrated circuit package? Draw a neat block diagram and label all the input and the output terminals in the ROM.

5. Design a 5 × 32 decoder using 3 × 8 decoder and summarize how many decoders are required for designing the circuit.

6. Explain the organization of ROM with suitable diagrams.

SECTION-C

7. A 5-bit D/A converter produces $V_{OUT} = 0.2V$ for, a digital input of 0001. Find the value of V_{out} for an input of 11111.

8. Write a program to implement a BCD to Excess–3 code conversion using a PLA.

9. Explain in detail about the working of bipolar SRAM cell and single transistor DRAM cell with neat sketches.